Entry approved HH 8/9/02

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 3204

PATENT APPLICATION
Do. No. 5038-062

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: John B. Halbert and Randy M. Bonella

Serial No.: 09/666,528 Examiner: Huan Hoang

Filed: September 18, 2000 Group Art Unit: 2818

For: MEMORY SYSTEM HAVING BUFFERS FOR ISOLATING STACKED MEMORY DEVICES

Date: July 22, 2002

BOX AF
Assistant Commissioner for Patents
Washington, DC 20231

RESPONSE TO FINAL OFFICE ACTION

Responsive to the Office Action, dated May 22, 2002, please amend the application as follows.

In The Claims

Please cancel claims 1, 2, 3, 4, 17 and 24 without prejudice.

Please amend claims 25-27 by rewriting as follows:

19.
25. (Amended once) A memory system comprising:

a bus;

a plurality of stacks of memory devices;

a buffer coupled between the plurality of stacks of memory devices and the bus;

a second plurality of stacks of memory devices; and

a second buffer coupled between the second plurality of stacks of memory devices and the bus.